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L Number	Hits	Search Text	DB	Time stamp
-	1306	205/118,125,131.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/25 17:26
-	568	205/118,125,131.ccls. and (hole or throughhole or "through-hole" or via)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/25 17:27
-	591	205/118,125,131.ccls. and (hole or throughhole or "through-hole" or via or cavity)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/25 17:29
-	89	205/118,125,131.ccls. and (aspect adj ratio)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/25 17:28
-	612	205/118,125,131.ccls. and (hole or throughhole or "through-hole" or via or cavity or passthrough or "pass through")	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/25 17:29
-	628	205/118,125,131.ccls. and (hole or throughhole or "through-hole" or via or cavity or passthrough or "pass through" or channel)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/25 17:29
-	83	(205/118,125,131.ccls. and (aspect adj ratio)) and (205/118,125,131.ccls. and (hole or throughhole or "through-hole" or via or cavity or passthrough or "pass through" or channel))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/25 17:30
-	16	205/118,125,131.ccls. and (pulse same (reverse or reversing))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/25 17:31
-	20	205/118,125,131.ccls. and ((pulse or pulsing) same (reverse or reversing))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/25 17:32
-	13	((205/118,125,131.ccls. and (aspect adj ratio)) and (205/118,125,131.ccls. and (hole or throughhole or "through-hole" or via or cavity or passthrough or "pass through" or channel))) and (205/118,125,131.ccls. and ((pulse or pulsing) same (reverse or reversing)))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/25 17:43
-	0	232862.apn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/25 17:44
-	0	232864.apn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/25 17:44

-	2	6391166.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/25 18:41
-	34578	205/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/25 18:41
-	384	205/$.ccls. and (aspect adj ratio)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/25 18:41
-	36	(205/$.ccls. and (aspect adj ratio)) and (205/$.ccls. and ((pulse or pulsing) near2 (reverse or reversing)))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/27 10:59
-	700	205/$.ccls. and (carrier or suppressor) and (electroplating or electroplate or electrodepositing)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/27 11:00
-	0	(205/$.ccls. and (carrier or suppressor) and (electroplating or electroplate or electrodepositing)) and ((poly adj (ethylene glycol)) or (polyethylene adj glycol)) and polyoxylalkylene	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/27 11:08
-	75	(205/$.ccls. and (carrier or suppressor) and (electroplating or electroplate or electrodepositing)) and ((poly adj (ethylene glycol)) or (polyethylene adj glycol) or polyoxylalkylene)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/27 11:08
-	86	(205/$.ccls. and (carrier or suppressor) and (electroplating or electroplate or electrodepositing)) and ((poly adj (ethylene glycol)) or (polyethylene adj glycol) or polyoxylalkylene or polyoxyalkylene)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/27 11:08
-	5	(205/$.ccls. and (carrier or suppressor) and (electroplating or electroplate or electrodepositing)) and ((poly adj (ethylene glycol)) or (polyethylene adj glycol)) and (polyoxylalkylene or polyoxyalkylene)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/27 14:15
-	87	205/$.ccls. and (leveler with brightener)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/27 11:13
-	117	(205/$.ccls. and ((leveler or leveling) with (brightener or brightening))) and (copper adj plating)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/27 11:14
-	84	((205/$.ccls. and ((leveler or leveling) with (brightener or brightening))) and (copper adj plating)) and (via or trough or channel or throughhole or hole or passthrough or "pass through" or passage or cavity)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/27 15:33
-	239	205/$.ccls. and ((leveler or leveling) with (brightener or brightening))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/27 13:50

-	63	(205/$.ccls. and (leveler with brightener)) and (copper adj plating)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/27 13:50
-	103	205/$.ccls. and ((pulse or pulsing) near2 (reverse or reversing))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/27 13:51
-	3	"6444110"	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/27 15:29
-	1	2001-072987.NRAN.	DERWENT	2003/01/27 14:15
-	537	205/103,123.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/27 15:32
-	598	205/103,105,123.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/27 15:32
-	288	205/103,105,123.ccls. and (via or trough or channel or throughhole or hole or passthrough or "pass through" or passage or cavity)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/27 15:34
-	71	(205/103,105,123.ccls. and (via or trough or channel or throughhole or hole or passthrough or "pass through" or passage or cavity)) and (aspect adj ratio)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/27 15:38
-	26	((205/103,105,123.ccls. and (via or trough or channel or throughhole or hole or passthrough or "pass through" or passage or cavity)) and (aspect adj ratio)) and ((reverse or reversed or reversing) with (pulse or pulsed or pulsing))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/01/27 15:38

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(54) ELECTRODEPOSITION OF METALS IN SMALL RECESSES USING MODULATED ELECTRIC FIELDS

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(63) Continuation-in-part of application No. 09/553,616, filed on Apr. 20, 2000, now Pat. No. 6,303,014, which is a continuation-in-part of application No. 09/172,299, filed on Oct. 14, 1998, now Pat. No. 6,203,684 and which is a continuation-in-part of application No. 09/239,811, filed on Jan. 29, 1999, now Pat. No. 6,210,555 and which is a continuation-in-part of application No. PCT/US99/23653, filed on Oct. 14, 1999.

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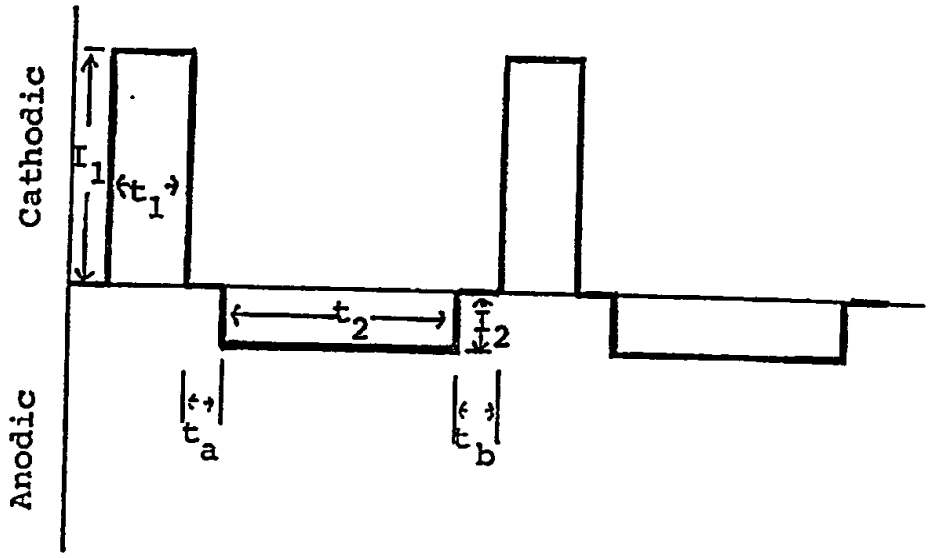
(57) **ABSTRACT**

A layer of a metal is electroplated onto an electrically conducting substrate having a generally smooth surface with a small recess therein, having a transverse dimension not greater than about 350 micrometers, typically from about 5 micrometers to about 350 micrometers, by immersing the substrate and a counterelectrode in an electroplating bath of the metal to be electroplated and passing a modulated reversing electric current between the electrodes. The current contains pulses that are cathodic with respect to said substrate and pulses that are anodic with respect to said substrate. The cathodic pulses typically have a duty cycle less than about 50% and the anodic pulses have a duty cycle greater than about 50%, the charge transfer ratio of the cathodic pulses to the anodic pulses is greater than one, and the frequency of the pulses ranges from about 10 Hertz to about 12000 Hertz. The on-time of the cathodic pulses may range from about 0.83 microseconds to about 50 milliseconds. The anodic pulse is longer than the cathodic pulse and may range from about 42 μs to about 99 milliseconds. The plating bath may be substantially devoid of levelers and/or brighteners.



[0168] Two slightly different plating baths were used having the following compositions:

[0169] Bath 1: 60-65 g/l $CuSO_4.5H_2O$; 50-60 parts per million (ppm) Cl^-; 350 ppm of polyethylene glycol (PEG) (average molecular weight, 200).

[0170] Bath 2: 60-65 g/l $CuSO_4.5H_2O$; 50-60 parts per million (ppm) Cl^-; 350 ppm of polyethylene glycol (PEG) (mixture of average molecular weights 200 and 1450).

[0171] The RDE was rotated at a speed of either 400 or 800 revolutions per minute (rpm)

[0172] Two different charge modulated electric field waveforms were used:

[0173] Waveform 1: 4000-5000 Hz, cathodic duty cycle 22% (cathodic on-time (t_c) 44-55 microseconds), anodic duty cycle 78% (anodic on-time (t_a) 156-195 microseconds), average cathodic current density (i_cD_c) about 30 amperes per square foot (ASF).

[0174] Waveform 2: 9000 Hz, cathodic duty cycle 40-45% (cathodic on-time (t_c) 44-61 microseconds), anodic duty cycle 55-60% (anodic on-time (t_a) 61-67 microseconds), average cathodic current density (i_cD_c) about 30 amperes per square foot (ASF)

[0175] The plating was conducted for periods ranging from 210 to 300 seconds as indicated below.

[0176] The experimental conditions are summarized in Table 2 below.

TABLE 2

Ex.	Trench width (μ)	Plating Bath	Rotation Speed (rpm)	Waveform	Time (sec)	Cathodic peak current (mA)	Anodic peak current (mA)	Applied Charge ratio Q_c Q_a
7	0.25	1	400	1	300	425	100	1.2
8	0.25	2	400	1	240	420	125	0.95
9	0.25 1.0	1	400	2	240	250	125	1.3
10	0.25	2	400	2	210	250	150–175	1.11
11	0.25	2	800	2	210	250	175	0.95

[0177] Cross sections of the trenches in the plated wafers were exposed by focused ion beam (FIB) excavation, and micrographs were prepared using a scanning electron microscope (SEM).

[0178] **FIG. 12** shows a cross-section of the plated trenches of Example 7. The trenches, having an aspect ratio of about 2, are fully filled and the thickness of the surface deposit is no greater than the depth of the trenches.

[0179] **FIG. 13** shows a cross-section of the plated trenches of Example 8. The trenches, having an aspect ratio of about 2, are conformally coated with a thin surface deposit.

[0180] **FIG. 14** shows a cross-section of the plated trenches of Example 9. The trenches, having widths of 0.25 micrometers and 1 micrometer and a depth of about 0.6-0.7 micrometer, are fully filled with a surface plating thickness significantly less than the depth of the trenches.

[0181] **FIG. 15** shows a cross-section of the plated trenches of Example 10. The surface plating is of moderate thickness.

[0182] **FIG. 16** shows a cross-section of the plated trenches of Examplell. The trenches have a conformal coating and the surface plating is thin.

EXAMPLE 12

[0183] This example illustrates filling of trenches having a width of about 10 micrometers.

[0184] Test coupons made from silicon wafers were prepared as in Examples 7-11, having V-shaped trenches having a top width of about 10 micrometers and a depth of about 5 micrometers. The coupons were plated in an apparatus similar to that used for Examples 7-11 for a period of 38 minutes in a bath similar to that of Example 7, using pulse reverse electric filed having a frequency of about 3500 Hz with excursions between about 2950 Hz and about 4969 Hz, a cathodic duty cycle of about 14.7%-16.7%, an anodic duty cycle of about 85.3%-83.3%, a cathodic on time of about 0.044-0.058 ms, a charge ration of about 1.16, a peak cathodic current of about 480 mA, an anodic peak current of about 80 mA, and an average current of about 11 mA. **FIG. 17** shows a cross-section of the plated trenches. The trenches are fully filled and the surface plating is much thinner than the depth of the trenches.

[0185] The invention having now been fully described, it should be understood that it may be embodied in other specific forms or variations without departing from its spirit or essential characteristics. Accordingly, the embodiments described above are to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are intended to be embraced therein.

We claim:

1. A method for depositing a continuous layer of a metal onto a substrate having small recesses in its surface comprising

immersing an electrically conductive substrate having a generally smooth surface having small recesses therein in an electroplating bath containing ions of a metal to be deposited onto said surface, said electroplating bath being substantially devoid of at least one member selected from the group consisting of levelers and brighteners,

immersing a counter electrode in said plating bath

passing an electric current between said electrodes,

wherein

said electric current is a modulated reversing electric current comprising pulses that are cathodic with respect to said substrate and pulses that are anodic with respect to said substrate,

the charge transfer ratio of said cathodic pulses to said anodic pulses is greater than one, and

the on-time of said cathodic pulses ranges from about 0.83 microseconds to about 50 milliseconds and the on-time of said anodic pulses is greater than the on-time of said cathodic pulses and ranges from about 42 microseconds to about 99 milliseconds.

2. The method of claim 1 wherein an interval of no electric current flow is interposed between said cathodic pulses and succeeding anodic pulses.

3. The method of claim 1 wherein an interval of no electric current flow is interposed between said anodic pulses and succeeding cathodic pulses.

4. The method of claim 1 wherein an interval of no electric current flow is interposed between said cathodic pulses and succeeding anodic pulses and between said anodic pulses and succeeding cathodic pulses.

5. The method of claim 1 wherein said cathodic pulses and said anodic pulses succeed each other without intervening intervals of no electric current flow.

6. The method of claim 1 wherein said cathodic pulses and said anodic pulses form a pulse train wherein the on-time of said cathodic pulses ranges from about 1 microsecond to about 10 milliseconds and the on-time of said anodic pulses is greater than that of said cathodic pulses and ranges from about 50 microseconds to about 19.8 milliseconds.

7. The method of claim 1 wherein said cathodic pulses and said anodic pulses form a pulse train wherein the on-time of said cathodic pulses ranges from about 1.7 microseconds to about 5 milliseconds and the on-time of said anodic pulses is greater than that of said cathodic pulses and ranges from about 84 microseconds to about 9.9 milliseconds.

8. The method of claim 1 wherein said cathodic pulses and said anodic pulses form a pulse train wherein the on-time of said cathodic pulses ranges from about 2.5 microseconds to about 1 millisecond and the on-time of said anodic pulses is greater than that of said cathodic pulses and ranges from about 125 microseconds to about 1.98 milliseconds.

9. The method of claim 1 wherein said cathodic pulses have a duty cycle of from about 30% to about 1%.

10. The method of claim 1 wherein said cathodic pulses have a duty cycle of from about 30% to about 15%.

11. The method of claim 1 wherein said cathodic pulses have a duty cycle of from about 30% to about 20%.

12. The method of claim 1 wherein said anodic pulses have a duty cycle of from about 60% to about 99%.

13. The method of claim 1 wherein said anodic pulses have a duty cycle of from about 70% to about 85%.

14. The method of claim 1 wherein said cathodic pulses have a duty cycle of from about 70% to about 80%.

15. The method of claim 1 wherein said metal is selected from the group consisting of copper, silver, gold, zinc, chromium, nickel, bronze, brass, and alloys thereof.

16. The method of claim 1 wherein a layer of metal of substantially uniform thickness is deposited on said surface and within said recesses.

17. The method of claim 1 wherein the thickness of the metal layer deposited within said recesses is greater than the thickness of the metal layer deposited on said surface.

18. The method of claim 1 wherein said recesses are substantially filled with metal.

19. The method of claim 1 wherein said recess has at least one transverse dimension not greater than about 350 micrometers.

20. The method of claim 1 wherein at least one transverse dimension of said recess is from about 5 micrometers to about 350 micrometers.

21. The method of claim 1 wherein at least one transverse dimension of said recess is from about 10 micrometers to about 250 micrometers.

22. The method of claim 1 wherein at least one transverse dimension of said recess is from about 25 micrometers to about 250 micrometers.

23. The method of claim 1 wherein at least one transverse dimension of said recess is from about 50 micrometers to about 150 micrometers.

24. A substrate having a surface with a small recess in said surface, said substrate having a layer of metal deposited in said recess and on said surface by the process of claim 1.

25. The substrate of claim 24 wherein said metal layer is of substantially uniform thickness on said surface and on interior surfaces of said recess.

26. The substrate of claim 24 wherein said recesses are filled with metal.

27. A multilayer high density interconnect structure having

a first interconnect layer and a second interconnect layer

said first interconnect layer having a first via substantially completely filled with metal, and

said second interconnect layer having a via positioned immediately above said first via,

said first and second interconnect layers having been prepared by the process of claim 1.

28. The method of claim 1 wherein said substrate has a microrough surface.

29. The method of claim 1 wherein said substrate is a semiconductor wafer.

30. The method of claim 1 wherein said semiconductor wafer has at lest one recess formed in its surface, said recess having at least one transverse dimension not greater than about 5 micrometers.

31. The method of claim 30 wherein said recess has at least one transverse dimension not greater than about 1 micrometer.

32. A semiconductor wafer having a microrough surface comprising surface areas and trenches formed therein, said microrough surface having a layer of metal deposited in said trenches and on said surface areas by the process of claim 1.

33. The semiconductor wafer of claim 32 wherein said metal layer on said surface areas has a thickness no greater than the depth of said trenches.

34. The semiconductor wafer of claim 32 wherein said metal layer on said surface areas has a thickness substantially less than the depth of said trenches.

35. The semiconductor wafer of claim 32 wherein said metal layer on said surface areas has a thickness no greater than about 50% of the depth of said trenches.

36. The semiconductor wafer of claim 32 wherein said metal layer on said surface areas has a thickness no greater about 20% of the depth of said trenches.

37. The semiconductor wafer of claim 32 wherein said metal layer on said surface areas has a thickness no greater than about 10% of the depth of said trenches.

38. The method of claim 1 wherein said plating bath is substantially devoid of brighteners.

39. The method of claim 1 wherein said plating bath is substantially devoid of levelers.

40. The method of claim 1 wherein said plating bath is substantially devoid of brighteners and levelers.

41. The method of claim 1 wherein said metal is copper and said plating bath contains a suppressor.

42. The method of claim 41 wherein said suppressor is present in an amount of from about 100 parts per million to about 5% by weight of said plating bath.

43. The method of claim 41 wherein said suppressor is present in an amount of from about 200 parts per million to about 800 parts per million by weight of said plating bath.

44. The method of claim 41 wherein said suppressor is present in an amount of about 300 parts per million of said plating bath.

45. The method of claim 41 wherein said suppressor is an organic polyhydroxy compound.

46. The method of claim 41 wherein said suppressor is poly(ethylene glycol).

47. The method of claim 46 wherein said poly(ethylene glycol) has a molecular weight in the range of from about 1000 to about 12000.

48. The method of claim 46 wherein said poly(ethylene glycol) has a molecular weight in the range of from about 2500 to about 5000.

49. The method of claim 1 wherein said cathodic pulses have a duty cycle less than about 50% and said anodic pulses have a duty cycle greater than about 50%.

50. A method for depositing a continuous layer of a metal onto a substrate having small recesses in its surface comprising immersing, as an electrode, an electrically conductive substrate having a generally smooth surface having small recesses therein in an electroplating bath containing ions of a metal to be deposited onto said surface, said electroplating bath being substantially devoid of at least one member selected from the group consisting of levelers and brighteners,

immersing a counter electrode in said plating bath

passing an electric current between said electrodes,

wherein

said electric current is a modulated reversing electric current comprising pulses that are cathodic with respect to said substrate and pulses that are anodic with respect to said substrate,

the charge transfer ratio of said cathodic pulses to said anodic pulses is greater than one, and

said cathodic pulses have an on-time and current density selected to produce electrodeposition under predominantly tertiary control and said anodic pulses have an on-time and current density selected to produce electroremoval of metal under predominantly primary and secondary control.

51. The method of claim 50 wherein said cathodic pulses have a duty cycle less than about 50% and said anodic pulses have a duty cycle greater than about 50%.

52. The method of claim 50 wherein an interval of no electric current flow is interposed between said cathodic pulses and succeeding anodic pulses.

53. The method of claim 50 wherein an interval of no electric current flow is interposed between said anodic pulses and succeeding cathodic pulses.

54. The method of claim 50 wherein an interval of no electric current flow is interposed between said cathodic pulses and succeeding anodic pulses and between said anodic pulses and succeeding cathodic pulses.

55. The method of claim 50 wherein said cathodic pulses and said anodic pulses succeed each other without intervening intervals of no electric current flow.

56. The method of claim 50 wherein said cathodic pulses and said anodic pulses form a pulse train wherein the on-time of said cathodic pulses ranges from about 1 microsecond to about 10 milliseconds and the on-time of said anodic pulses is greater than that of said cathodic pulses and ranges from about 50 microseconds to about 19.8 milliseconds.

57. The method of claim 50 wherein said cathodic pulses and said anodic pulses form a pulse train wherein the on-time of said cathodic pulses ranges from about 1.7 microseconds to about 5 milliseconds and the on-time of said anodic pulses is greater than that of said cathodic pulses and ranges from about 84 microseconds to about 9.9 milliseconds.

58. The method of claim 50 wherein said cathodic pulses and said anodic pulses form a pulse train wherein the on-time of said cathodic pulses ranges from about 2.5 microseconds to about 1 millisecond and the on-time of said anodic pulses is greater than that of said cathodic pulses and ranges from about 125 microseconds to about 1.98 milliseconds.

59. The method of claim 50 wherein said cathodic pulses have a duty cycle of from about 30% to about 1%.

60. The method of claim 50 wherein said cathodic pulses have a duty cycle of from about 30% to about 15%.

61. The method of claim 50 wherein said cathodic pulses have a duty cycle of from about 30% to about 20%.

62. The method of claim 50 wherein said anodic pulses have a duty cycle of from about 60% to about 99%.

63. The method of claim 50 wherein said anodic pulses have a duty cycle of from about 70% to about 85%.

64. The method of claim 50 wherein said cathodic pulses have a duty cycle of from about 70% to about 80%.

65. The method of claim 50 wherein said metal is selected from the group consisting of copper, silver, gold, zinc, chromium, nickel, bronze, brass, and alloys thereof.

66. The method of claim 50 wherein a layer of metal of substantially uniform thickness is deposited on said surface and within said recesses.

67. The method of claim 50 wherein the thickness of the metal layer deposited within said recesses is greater than the thickness of the metal layer deposited on said surface.

68. The method of claim 50 wherein said recesses are substantially filled with metal.

69. The method of claim 50 wherein said recess has at least one transverse dimension not greater than about 350 micrometers.

70. The method of claim 50 wherein at least one transverse dimension of said recess is from about 5 micrometers to about 350 micrometers.

71. The method of claim 50 wherein at least one transverse dimension of said recess is from about 10 micrometers to about 250 micrometers.

72. The method of claim 50 wherein at least one transverse dimension of said recess is from about 25 micrometers to about 250 micrometers.

73. The method of claim 50 wherein at least one transverse dimension of said recess is from about 50 micrometers to about 150 micrometers.

74. A substrate having a surface with a small recess in said surface, said substrate having a layer of metal deposited in said recess and on said surface by the process of claim 50.

75. The substrate of claim 74 wherein said metal layer is of substantially uniform thickness on said surface and on interior surfaces of said recess.

76. The substrate of claim 74 wherein said recesses are filled with metal.

77. A multilayer high density interconnect structure having

a first interconnect layer and a second interconnect layer

said first interconnect layer having a first via substantially completely filled with metal, and

said second interconnect layer having a via positioned immediately above said first via,

said first and second interconnect layers having been prepared by the process of claim 50.

78. The method of claim 50 wherein said substrate has a microrough surface.

79. The method of claim 50 wherein said substrate is a semiconductor wafer.

80. The method of claim 50 wherein said semiconductor wafer has at lest one recess formed in its surface, said recess having at least one transverse dimension not greater than about 5 micrometers.

81. The method of claim 80 wherein said recess has at least one transverse dimension not greater than about 1 micrometer.

82. A semiconductor wafer having a microrough surface comprising surface areas and trenches formed therein, said microrough surface having a layer of metal deposited in said trenches and on said surface areas by the process of claim 50.

83. The semiconductor wafer of claim 82 wherein said metal layer on said surface areas has a thickness no greater than the depth of said trenches.

84. The semiconductor wafer of claim 82 wherein said metal layer on said surface areas has a thickness substantially less than the depth of said trenches.

85. The semiconductor wafer of claim 82 wherein said metal layer on said surface areas has a thickness no greater than about 50% of the depth of said trenches.

86. The semiconductor wafer of claim 82 wherein said metal layer on said surface areas has a thickness no greater about 20% of the depth of said trenches.

87. The semiconductor wafer of claim 82 wherein said metal layer on said surface areas has a thickness no greater than about 10% of the depth of said trenches.

88. The method of claim 50 wherein said plating bath is substantially devoid of brighteners.

89. The method of claim 50 wherein said plating bath is substantially devoid of levelers.

90. The method of claim 50 wherein said plating bath is substantially devoid of brighteners and levelers.

91. The method of claim 50 wherein said metal is copper and said plating bath contains a suppressor.

92. The method of claim 91 wherein said suppressor is present in an amount of from about 100 parts per million to about 5% by weight of said plating bath.

93. The method of claim 91 wherein said suppressor is present in an amount of from about 200 parts per million to about 800 parts per million by weight of said plating bath.

94. The method of claim 91 wherein said suppressor is present in an amount of about 300 parts per million of said plating bath.

95. The method of claim 91 wherein said suppressor is an organic polyhydroxy compound.

96. The method of claim 91 wherein said suppressor is poly(ethylene glycol).

97. The method of claim 96 wherein said poly(ethylene glycol) has a molecular weight in the range of from about 1000 to about 12000.

98. The method of claim 96 wherein said poly(ethylene glycol) has a molecular weight in the range of from about 2500 to about 5000.

* * * * *